UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/986,742	11/09/2001	Jun Koyama	740756-2384	5965

22204 7590 07/30/2003

NIXON PEABODY, LLP
8180 GREENSBORO DRIVE
SUITE 800
MCLEAN, VA 22102

EXAMINER
ECKERT II, GEORGE C

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/986,742	Koyama
Examiner	**Art Unit**
George C. Eckert II	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *May 27, 2003* .

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-6 and 15-28* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-6 and 15-28* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *May 29, 2003* is/are a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Amendment

1. Applicant's amendment dated May 27, 2003 canceling claims 7-14 has been entered.

Drawings

2. The corrected drawings were received on May 29, 2003. These drawings are acceptable.

Specification

3. Objection to the disclosure is overcome by applicant's amendment.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,365,875 to Asai et al. Asai et al. teach, with reference to column 8 lines 18-43, a semiconductor device comprising:

a thin film transistor (e.g. figure 7(g)) comprising a polycrystalline semiconductor layer (e.g. 14, figure 7(d), col. 7, lines 46-49),

wherein a gate length of the thin film transistor is 10 μm (greater than 7μm) and the gate width is 50μm (col. 8, line 29).

The limitations that the transistor is used in a buffer circuit or a lcd based device are considered an intended use of the transistor structure and do not serve to further limit the structure of the instant claims. Moreover, Asai et al. teach that the transistor may be used in liquid crystal panels or contact type image sensors (col. 1, lines 13-16).

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 15, 16, 19, 20, 22, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's prior art as shown in figure 5, in view of Asai et al. Applicant's prior art teaches the various circuit arrangements as instantly claimed including current mirror and differential circuits. However, the prior art does not teach that the circuits use transistors having a gate length of 7 μm or greater or a gate width of 50 μm or greater. Asai et al. teach a transistor having the claimed gate dimensions.

Applicant's prior art and Asai et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the transistors of Asai et al. in the device of Applicant's admitted prior art. The

motivation for doing so, as it taught by Asai et al., is that transistors having such dimensions and formed as taught by Asai et al. have uniform crystallinity in the semiconductor layer (col. 2, lines 5-13). Therefore, it would have been obvious to combine Applicant's prior art with Asai et al. to obtain the invention of claims 15, 16, 19, 20, 22, 25 and 26.

6. Claims 17, 18, 21, 23, 24, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's prior art in view of Asai et al. and further in view of Dabral et al. As discussed immediately above, Applicant's prior art and Asai et al. make obvious a device having the instantly claimed circuit configuration and transistor gate dimensions. However, it is not made obvious by either reference that the transistor have a multi-gate. Dabral et al. teach, with reference to figure 2, a transistor having a multi-gate.

Applicant's prior art and Asai et al. are combinable with Dabral et al. because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to further modify the device of Applicant's prior art and Asai et al. to have a multi-gate as taught by Dabral et al. The motivation for doing so, as is taught by Dabral et al., is that the use of a multi-gate structure will reduce the affect of processing variations in like devices (col. 3, lines 6-8). Therefore, it would have been obvious to combine Asai et al. with Dabral et al. to obtain the invention of claims 17, 18, 21, 23, 24, 27 and 28.

Response to Arguments

7. Applicant's arguments filed May 27, 2003 have been fully considered but they are not persuasive. Applicant first argues that the rejection of claims 1-6 over Asai must fail because an "analog buffer" is a structural limitation not taught by Asai. However, this is not persuasive. A buffer circuit may comprise a single transistor such that the recitation is no more than functional or intended use language. This is supported by applicant's claim language which states "an analog buffer comprising *at least one* thin film transistor" (*emphasis added*). Also, applicant has merely argued that Asai does not teach the claimed structure but has not pointed out what structure is required of a buffer circuit beyond that taught by Asai. In all, the argument is not persuasive and the rejection is maintained.

Regarding the rejection of claims 15, 16, 19, 20, 22 25 and 26 over applicant's prior art in view of Asai, applicant argues first that Asai does not teach an analog buffer. As discussed above, this argument is not persuasive as an analog buffer may be comprised of the single transistor of Asai. Applicant also argues that motivation is lacking in the admitted prior art for combining the admitted prior art with Asai and that the rejection is based on hindsight. However, as pointed out in the above rejection, Asai provides express motivation for its combination with the prior art. As such, the assertion of hindsight is unfounded and the rejection is maintained.

Applicant also argues the rejection of claims 17, 18, 21, 23, 24, 27 and 28, asserting the rejection lacks motivation. However, again as pointed out in the above rejection, both Asai and Dabral provide motivation for their combination and the rejection is proper.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (703) 305-2752.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Eddie Lee can be reached on (703) 308-1690. The fax number is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

GCE
July 28, 2003

GEORGE ECKERT
PRIMARY EXAMINER